**Systolic Array Based Processor**

**Monthly Progress Report (1/2/2016 to 29/2/2016)**

* Coding and testing of MAC, Adder, Shift register modules: The following units were coded in VHDL and their outputs were tested on a testbench: MAC Unit, adder, shift register.
* Coding and testing of the individual DPU: The individual DPU was coded in VHDL. An individual DPU consists of the MAC unit, adder modules and shift registers which were implemented and tested in the previous stage. A simple and custom architecture of the DPU was chosen for faster implementation.
* VHDL coding and testing of interconnects between DPU’s: In order to implement the systolic array of processors (DPUs), the interconnects between the DPUs were coded and tested on VHDL.
* RTL synthesis of 3 \* 3 matrix architecture: Followed by the successful testing of the interconnects, an RTL synthesis of a basic 3\*3 matrix structure consisting of 9 DPUs was done. Each of the 9 DPUs were connected to the adjacent DPUs in order to ensure proper data flow.
* Debugging and optimization of the codes: The various codes that were written in the previous stages were optimized for faster run time and better integration. Minor errors in the codes that was left unnoticed during the initial coding phase was debugged and clarified for the integration of the DPUs.
* Testbench simulation of 3 \* 3 matrix DPU architecture: The testing of the 3\*3 systolic array of processors was done on the testbench in VHDL. A 4 bit matrix multiplication was implemented and the waveforms were analysed.

**Work Scheduled to be done (1/3/2016 to 15/3/2016)**

* I2C interface design between Raspberry-Pi and FPGA: In order to access memory for the interconnects, a Raspberry Pi has to be used. The communication between the FPGA and the Pi is done using the I2C interface protocol.

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